



## Sales Brief

# There is a Server Platform Chipset Optimized for the Intel® Xeon™ Processor with 533 MHz System Bus

The Intel® E7501 chipset represents Intel's continuing commitment to world-class chipsets for server platforms and has been designed to take full advantage of the latest system bus speeds of the Intel® Xeon™ processor.

## Next-Generation Server Chipset Technology

Optimized for the Intel® Xeon™ processor with 533 MHz system bus and Intel® NetBurst™ microarchitecture, the Intel® E7501 chipset is an ideal solution for dual-processor (DP)-based servers—delivering performance, flexibility, and expandability for a new generation of volume DP-based servers.

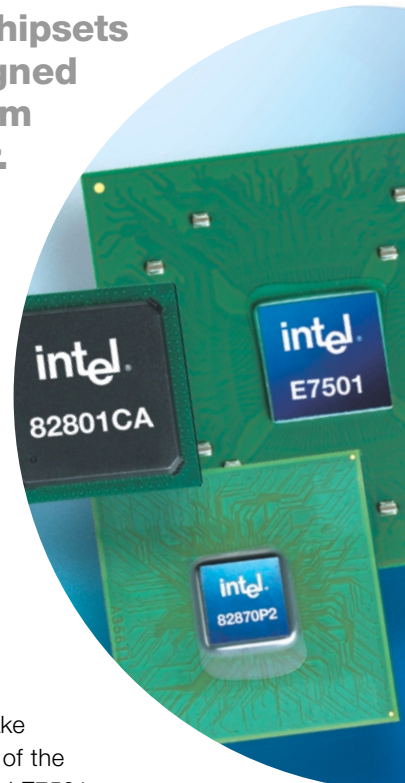
## New Features Deliver Greater Performance

**Latest Server Processors:** The Intel E7501 chipset takes full advantage of the Intel Xeon processor by enabling a platform that delivers 4.3 GB/s of bandwidth across the 533 MHz system bus interface, thereby providing more performance headroom for peak server workloads.

**Enhanced Memory:** A high-bandwidth memory subsystem is vital to take full advantage of the faster system bus and advanced I/O capabilities of the Intel Xeon processor-based server with the Intel E7501 chipset. The Intel E7501 Memory Controller Hub (MCH) enhances server platforms by using a 144-bit wide, 266 MHz Double Data Rate (DDR) SDRAM interface to deliver a maximum memory bandwidth of 4.3 GB/s. Four DIMMs per channel (eight DIMMs total) allow a maximum memory configuration of 16 GB with 512 Mb device densities.

**Flexible I/O Options:** Up to three Intel® 82870P2 64-bit PCI/PCI-X Controller Hub 2.0 devices can connect to the MCH, each providing a maximum bandwidth greater than 1 GB/s for a total of 3.2 GB/s of I/O bandwidth. Each controller hub contains two independent, 64-bit, 133 MHz PCI-X interfaces and two PCI hot-plug controllers. For added I/O configuration flexibility, the Intel® 82545EM Gigabit Ethernet or Intel® 82546EB dual Gigabit Ethernet controllers and Intel® IOP321 I/O processors can attach to the Intel 82870P2 controller hub.

**Legacy Compatibility:** The Intel® 82801CA I/O Controller Hub provides legacy I/O interfaces through integrated features such as a two-channel Ultra ATA/100 bus master IDE controller, three USB controllers (for up to six total USB 1.0 ports), and a 32-bit PCI interface. The Intel 82801CA I/O controller hub also offers a System Manageability Bus controller, an integrated LAN controller, as well as AC'97 2.2-compliant and PCI 2.2-compliant interfaces.



**The Intel® E7501 Chipset delivers performance, stability, and value for volume DP-based servers.**



The features provided by both the Intel Xeon processor for DP-based servers and the Intel E7501 chipset enable the delivery of stable technology for today's demanding business solutions. Paired with the Intel Xeon processor and revolutionary Intel NetBurst microarchitecture, the innovative design of the Intel E7501 chipset delivers maximized system bus, memory and I/O bandwidth to optimize performance, scalability, and end-user productivity, while providing a solid base for future technology.

The diagram illustrates the system architecture of the Intel® Xeon™ E7501 (MCH). At the center is the Intel® E7501 (MCH) block. It is connected to two Intel® Xeon™ Processors (green boxes) above it, each with a 533 MHz / 4.3 GB/s connection. To the left, it connects to an Intel® 82801CA block (blue box) with a 266 MB/s / 8-bit / HI 1.5 connection. To the right, it connects to memory modules (pink boxes) with a 4.3 GB/s connection. The memory configuration is specified as 2 Channels, 266 MHz DDR, 4 DIMMs/Ch, Intel® x4 Single Device Data Correction\*\*, ECC, and 16 GB Max Memory. Below the MCH, it connects to three Intel® 82870P2 blocks (yellow boxes) with 1.066 GB/s connections. Each 82870P2 block is connected to two PCI-X ports (red boxes) via a Hot-Plug connection, with a 16-bit HI 2.0 connection specified for the middle 82870P2 block.

```

graph TD
    P1[Intel® Xeon™ Processor] ---|533 MHz  
4.3 GB/s| MCH[Intel® E7501 (MCH)]
    P2[Intel® Xeon™ Processor] ---|533 MHz  
4.3 GB/s| MCH
    MCH ---|266 MB/s  
8-bit  
HI 1.5| I82801CA[Intel® 82801CA]
    MCH ---|4.3 GB/s| Mem[2 Channels  
266 MHz DDR  
4 DIMMs/Ch  
Intel® x4  
Single Device  
Data  
Correction**  
ECC  
16 GB Max  
Memory]
    MCH ---|1.066 GB/s| P3[Intel® 82870P2]
    MCH ---|1.066 GB/s| P4[Intel® 82870P2]
    MCH ---|1.066 GB/s| P5[Intel® 82870P2]
    P3 ---|Hot-Plug| PCI1[PCI-X]
    P3 ---|Hot-Plug| PCI2[PCI-X]
    P4 ---|Hot-Plug| PCI3[PCI-X]
    P4 ---|Hot-Plug| PCI4[PCI-X]
    P5 ---|Hot-Plug| PCI5[PCI-X]
    P5 ---|Hot-Plug| PCI6[PCI-X]
    P4 -.-|16-bit HI 2.0| P5
  
```

```

graph TD
    subgraph Left_Controller [Intel® 82870P2]
        direction TB
        L1[ ] --- L2[ ]
        L2 --- L3[ ]
        L3 --- L4[ ]
    end
    subgraph Right_Controller [Intel® 82870P2]
        direction TB
        R1[ ] --- R2[ ]
        R2 --- R3[ ]
        R3 --- R4[ ]
    end
    L1 --- L2[PCI-X]
    L2 --- L3[ ]
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    R1 --- R2[PCI-X]
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\*\*In a x4 DDR memory device, the Intel® x4 Single Device Data Correction (x4 SDDC), provides error detection and correction for 1, 2, 3, or 4 data bits within that single device and provides error detection, up to 8 data bits, within two devices.

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